Digital Design Laboratory
Checkoff Sheet

Lab 1

Lab Section:	
Student's Name (print):	

TA	Date & Time	Late?*	Description
			From Prelab Step 4: Schematic with title block
			From Lab Step 4: Functional simulation
			From Lab Step 5: Timing simulation
			From Lab Step 6: Circuit demonstration
			From Lab Step 7: First page of a chip datasheet

* This column is marked only by the GTA during grading, based on the Date & Time entry.

Check-off sheet goes on top

Lab Report Evaluation Sheet
ECE 2031: Digital Design Laboratory

Student's Name George Burdell Lab Section L12

Pledge of Academic Honesty: *On my honor, I pledge that I have neither given anyone else assistance or information on this lab report nor have I received assistance or information from anyone other than instructors or course teaching assistants. I pledge that I am in full compliance of the Georgia Tech Honor Code and that all of th y own, unless it is attributed to another source. I understand and agree that any violatio ill be forwarded to the Office of Student Integrity.*

Student's Signature George B

Date 01/01/1970

Filled-out evaluation sheet is second (download from UPCP site)

Grading Rubric: 150 points

Technical Content and Accuracy Points awarded for technically correct information.	**/80**
Effective Communication Points awarded for presenting information in an effective way, including both figures and captions.	**/50**
Proper Formatting Points awarded for proper formatting of the report and results.	**/20**
Final Score =	**/150**

Graduate TA signature: _____

Comments:

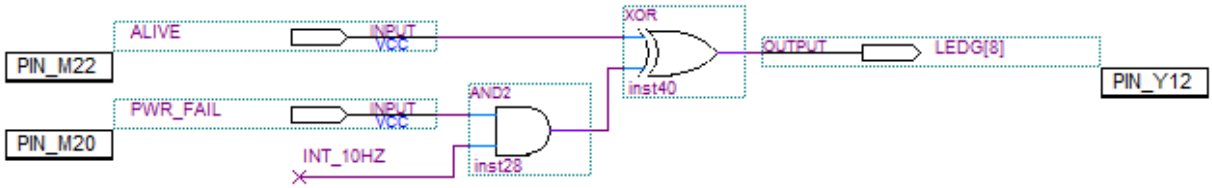

Figure 1. Circuit to light LED G8 when robot motors are enabled, and flash it at 10Hz when robot battery voltage is below minimum threshold.

```
-- DIG_IN.VHD (a peripheral module for SCOMP)
-- This module reads digital inputs directly, without debouncing
```

The rest of the document is results, formatted according to guidelines on UPCP site.

(note: these examples are NOT actual lab 1 results)

```
                                        IC;
                                        IC_VECTOR(15 DOWNTO 0);
                                        LOGIC_VECTOR(15 DOWNTO 0)
);
END DIG_IN;

ARCHITECTURE a OF DIG_IN IS
  SIGNAL B_DI : STD_LOGIC_VECTOR(15 DOWNTO 0);
  BEGIN
  -- Use LPM function to create bidirectional
  IO_BUS: lpm_bustri
  GENERIC MAP (
    lpm_width => 16
  )
  PORT MAP (
    data     => B_DI,
    enabledt => CS,
    tridata  => IO_DATA
  );
  B_DI <= DI;
END a;
```

Notice that the figure titles are detailed and self-contained. Be sure to check the figure title tips given on the UPCP

Figure 2. VHDL code to interface general-purpose digital inputs to SCOMP's I/O bus.