ECE 2031 Lab Report Content Requirements

This document lists the required results for each lab report in ECE 2031, and each result's contribution to the technical category of the lab report grade.

Each lab has an associated check-off sheet, and most (but not all) check-offs have an associated result that is included in the lab report. Only those results are detailed in this document, because check-offs with no associated result are graded solely based on the check-off being completed.

Some check-offs are prerequisites of later check-offs, and if a prerequisite check-off is missing, any dependent check-offs and their associated results, even if present, will not be graded.

Results specified in this document as *unformatted* should simply be stapled in the lab report in the order shown. They do not require figure captions, do not belong in appendices, and do not count towards the "formatting" or "effectiveness" grading categories.

Lab 1

Required result(s)	**Points**
Schematic for the circuit from prelab step 4.	24
Functional simulation results from lab step 4. [1]	20
Timing simulation results from lab step 5. [1]	20
Pinout page of the datasheet for one of the chips from lab step 7. *Unformatted.*	8

[1] Take a screenshot of simulation results within Quartus. Do not export them as images using Quartus's export function, because that will not include some required information, such as signal types.

Lab 2

Required result(s)	**Points**
Solved K-maps from prelab step 3. *Unformatted.*	20
Computer-annotated schematic diagram from lab step 14.	20
Oscilloscope trace capture from lab step 13. [1]	8

[1] Ensuring that oscilloscope screenshots are legible may require some post-capture image manipulation, such as inverting colors.

Lab 3

Required result(s)	Points
Table of propagation delays from prelab step 3.	12
Schematic with worst-case path from prelab step 4. [1]	12
Truth table with two highlighted rows from prelab 6. [1]	12
Tri-state circuit schematic from prelab step 13.	10
Oscilloscope screen captures of period and duty cycle (two figures) from lab step 7. [2]	5 each
Oscilloscope screen captures of rise time, fall time, and low-to-high and high-to-low propagation delay (four figures) from lab step 14. [2]	5 each

[1] If there are multiple correct options for a result (specifically here: multiple worst-case paths and/or multiple row pairs), choose one for all lab work.

[2] Correct measurement technique is part of these results. Possible errors include improper oscilloscope triggering, improper trace scaling, and incorrect measurement points.

Lab 4

Required result(s)	Points
Solved K-maps and state machine diagrams from prelab step 5. [1] *Unformatted.*	20
Circuit schematic from lab step 7 (originally from prelab step 7, annotated in lab step 7).	16
Simulation input waveform from lab step 4.	12
Simulation output and comparison waveform from lab step 6.	12

[1] Technical errors for state machine diagrams include missing or mis-labeled connections and missing or improperly formatted diagram features.

Lab 5

Required result(s)	Points
SM_VHDL.VHD file from prelab step 6, fixed if necessary in lab step 7.	12
SM_VHDL.VWF file from prelab step 16, reopened and saved as a screen capture.	12
Schematic after replacement of SM_VHDL with SM_SCHEMATIC (from lab step 9). [1]	16
Two logic analyzer screen captures from lab steps 18h and 18i	12 each

[1] For all schematic design files in ECE 2031, add a title block, or edit the existing title block to include your name.

Lab 6

Required result(s)	Points
Neatly handwritten train worksheets of final solution from lab step 10. *Unformatted.*	8
TCONTROL.VHD file from Lab step 10 [1]	12
Computer drawn UML diagram from Lab step 11. [1] [2]	20

[1] If you are unable to get the train controller to work correctly, you will not get credit for the second check-off or the VHDL, resulting in a loss of 28 points. However, as long as you update your worksheets and UML diagram to reflect your final (non-working) solution, **get the third check-off**, and those will still be graded.

[2] Improper construction of the UML diagram (such as missing transition events or entry point) are counted as technical errors.

Lab 7

Required result(s)	Points
Modified EXAMPLE.MIF from prelab step 3. [1]	12
Simulation waveform from prelab step 5.	16
TEST_CODE.MIF simulation waveform from lab step 2.	12
Schematic from lab steps 4-7 with title block added.	16
Oscilloscope waveform from lab step 8.	8

1 Open MIF files in a text editor, such as Notepad, and either screenshot or copy-paste the text to your results. Do not open MIF files in Quartus for your results.

Lab 8

Required result(s)	Points
Assembly language file and resulting MIF file from prelab step 4.	6 each
Simulation of the same program, using subroutine CALC from prelab step 8.	12
TOP_SCOMP.BDF file with connected clock signal from lab step 5. [1]	8
SCOMP.VHD included in the project with CALL, RETURN, IN, OUT, SHIFT, and modifications needed to support logic analyzer from lab step 5.	20
Assembly language file and the resulting MIF that implements Figure 8.18 from lab step 7.	12
Disassembled waveform from lab step 16 (trigger point and 2-4 instructions).	8
Disassembled listing from lab step 19 (trigger point and a dozen or two instructions).	8

[1] Crop to the area with the PLL and SCOMP, even though it cuts out the title block.